# APPLICATIONS OF PROGRAMMABLE RESISTANCE CHANGES IN METAL-DOPED CHALCOGENIDES

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## ABSTRACT

We describe the fundamental physical and electrical characteristics of two-terminal devices fabricated using thin films of metal-doped chalcogenides and discuss their potential applications in electronic systems. The basic device structure consists of two electrodes in contact with the chalcogenide layer. Certain dissolved metal ions are mobile in chalcogenides but the resistivity of the solid solution is many orders of magnitude higher than the solid metal. If an appropriate voltage is applied between the electrodes, the metal ions will come out of solution to form an electrodeposit between them. This voltage-induced connection and the ensuing resistance change can be used in a variety of applications in electronics, including programmable read only memories (PROMs), field configurable connections, and self-repairing interconnections. In this paper we report the results of our research on devices with coplanar electrodes which use an arsenic sulfide-silver ternary as the solid solution. The metal is added to arsenic trisulfide by photodissolution to form a saturated solid solution, close to the composition $Ag_4As_2S_3$. In addition to the dissolved metal, a layer containing silver is incorporated at the anode to act as a supply of metal ions during growth of the metal link so that electrodeposition does not become limited by reduced ion concentration.

## INTRODUCTION

It is well known in the field of electrochemistry that metals such as silver or copper can be dissolved in chalcogenide glasses such as arsenic sulfide or germanium selenide, to form solid solutions. These solid solutions are relatively poor conductors, with resistivity in excess of $10^8$ times higher than that of the solid metal, as conduction is dominated by ion transport through the solid electrolyte. If electrodes are formed in contact with a layer of the solid solution and a voltage is applied between them, the positively charged metal ions will migrate toward the cathode region. Under appropriate conditions, the ions will come out of solution at the cathode to form a stable metallic electrodeposit which may be made to extend from the cathode to the anode. The electrodeposit can form on the surface of the chalcogenide or through a thin layer of the glass, depending on the placement of the electrodes. In either case, the low resistance metal electrodeposit acts to short-out the relatively high resistance glass and hence the overall resistance of the structure can be reduced by many orders of magnitude via this electrically-stimulated deposition process. This is the basis of the Programmable Metallization Cell (PMC) technology [1]. In our work to date, we have concentrated on arsenic sulfide-silver ($As_2S_3$-Ag, $AsS_2$-Ag) and germanium selenide-silver ($GeSe_2$-Ag, $Ge_3Se_7$-Ag) systems [2]. We have also investigated copper as the dissolved metal

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species, albeit to a lesser degree. In this paper, we will concentrate on results from the arsenic trisulfide-silver ($As_2S_3$-Ag) system and on devices which have been fabricated with coplanar electrodes on the chalcogenide film. We are currently exploring three main application areas of the PMC technology: (1) low voltage/low power programmable read only memories, (2) field configurable connections, and (3) self-repairing interconnections. These applications will also be briefly discussed.

## FUNDAMENTAL MECHANISMS

In the work described in this paper, the silver is added to the $As_2S_3$ by photodissolution after the glass is deposited as a thin film on the substrate. This process involves the illumination of a metal/glass bilayer with light of energy greater than the optical gap of the chalcogenide (approximately 2.5 eV for undoped $As_2S_3$) [3]. The amount of metal dissolved in the film depends on the initial thickness of the metal layer and the illumination dose. The incorporation of the metal results in the reduction of the arsenic in the film. The dissolution process is thought to be self-limiting, halting when the arsenic has been reduced from the $3^+$ state to the $1^+$ state [4]. This occurs at a ternary composition of $Ag_4As_2S_3 = 2Ag_2S + As_2S$, which corresponds to a silver concentration of 44.4 at. %. This concentration has been confirmed in our films using Rutherford Backscattering Spectrometry (RBS) [2]. Silver concentration is apparently maintained in the film even as metal comes out of solution during electrodeposition if there is a source of metallic silver at the anode. The silver from the anode dissolves into the glass and moves toward the growing electrodeposit by a coordinated motion of the ions. This replacement of metal appears to be necessary for rapid and stable electrodeposit formation for the reasons discussed below.

The electrochemical deposition of silver from arsenic sulfide-silver glasses has been reported by other researchers in the past [5–8] but a complete understanding of this solid phase growth process has been somewhat elusive. The deposition of Ag metal at the cathode and partial dissolution of the Ag at the anode indicates that device operation is analogous to the reduction-oxidation electrolysis of metal from an aqueous solution. When an electrical bias is induced across an electrolytic cell, the anode will oxidize if the oxidation potential of the metal anode is greater than that of the solution. Under steady state conditions, as current flows in the cell, the metal ions will be reduced at the cathode. For a solid solution of silver in arsenic sulfide with silver electrodes, the reactions are:

$$\text{Anode: } Ag \rightarrow Ag^+ + e^-$$

$$\text{Cathode: } Ag^+ + e^- \rightarrow Ag.$$

When a potential is applied across the electrodes, silver ions migrate from the anode toward the cathode under the driving force of the applied electrical potential and the concentration gradient. This ion transport through the electrolyte can easily be the rate limiting factor in the electrodeposition process. At the boundary layer between the electrolyte and the electrodes, a finite potential difference exists due to the transfer of charge and change of state associated with the electrode reactions. This potential difference leads to polarization in the region close to the phase boundary (the electric double layer). When an external voltage is applied across the electrodes, current will

flow in order to charge the double layer, without causing any reduction or oxidation of the metal. An important consequence of the electric double layer is that for the redox reaction to proceed, the applied potential must overcome this double layer potential.

If the Ag anode is replaced with a metal with a lower oxidation potential than the solid solution, the anode will be essentially chemically inert and only serve as an electronic conduction path. The reduction of the metal ions in solution at the cathode will then occur at the expense of the solution. The concentration of $Ag^+$ in the solid solution will decrease during electrodeposition on the cathode until the electrode potential equals the applied potential and reduction will then be halted. Further reduction requires greater applied voltage (governed by the Nernst equation), so that the electrolytic deposition process is self limiting for a moderately low applied potential. This has important consequences for PMC device operation as the "stalled" electrodeposit may not bridge the electrode gap and hence the resistance of the device will remain high. In addition, the metal depleted glass could result in the subsequent thermal dissolution of the electrodeposit, which would not occur if the glass was maintained at the metal saturation point through dissolution of a silver anode.

Finally, it should be noted that the electrodeposition is reversible by the application of a reverse bias. If the electrodeposit itself is made the anode, it will dissolve back into the chalcogenide as metal comes out of solution at the opposite electrode.

## ELECTRICAL CHARACTERISTICS

The electrical characteristics of the PMC metal/solid solution/metal arrangement are complex but may be represented by a number of models. The a.c. equivalent circuit modeling which was performed by our group has been described elsewhere [9] so we will concentrate here on the d.c. characteristics in the sub-electrodeposition and electrodeposition regimes. We will also restrict our comments to results from devices which have coplanar electrodes, a configuration shown schematically in Fig. 1. These test

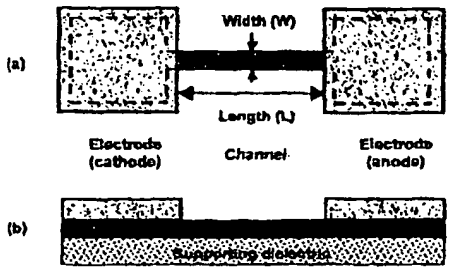


Fig. 1. Schematic diagram of coplanar electrode device. (a) Plan view, (b) side elevation.

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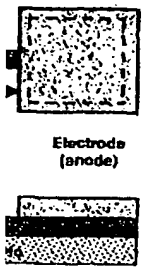


le device. (a) Plan view, (b)

devices were fabricated as follows. Thermal silicon dioxide (around 200 nm thick) was grown on silicon wafers to form the supporting dielectric layer for the devices. Positive photoresist was then deposited, exposed and developed to form the pattern for the chalcogenide layer. Undoped $As_2S_3$, 40 nm thick, was then evaporated from a powder source onto the patterned resist and this was immediately coated with a 25 nm thick layer of silver, without breaking the vacuum in the deposition system. The wafers were then removed and exposed with u.v. light at 436 nm for 10 minutes to fully saturate the chalcogenide and form the $Ag_4As_2S_3$ final composition (confirmed by RBS). Note that 25 nm of silver will leave around 2.4 nm of metallic silver on the surface of a 40 nm thick layer of $As_2S_3$ after photodoping is complete. The excess silver helps to ensure that saturation of the chalcogenide occurs. The doped chalcogenide is then patterned by lift-off. The large silver contacts (typically 100 x 100 μm and 150 nm thick) are also deposited by evaporation and patterned by lift-off. The devices are then passivated with a layer of Novolac resin which is baked at 120 °C for 20 minutes (this is the same as the resist hard bake step). The bake also serves to anneal the contacts and reduce the resistive effects of any interfacial layers.

The small-signal current vs. voltage (I-V) plot of a typical large geometry device is shown in Fig. 2 [10]. This plot appears similar to that which would be obtained from back-to-back Schottky contacts with a series resistance component which limits the current for applied potentials in excess of a few tens of mV. Applied potentials below 10 - 15 mV are insufficient to cause significant electrodeposition (see later) and in this range the I-V characteristics of the device are essentially governed by the classic Butler-Volmer equation, which relates current and applied voltage by an exponential relationship.

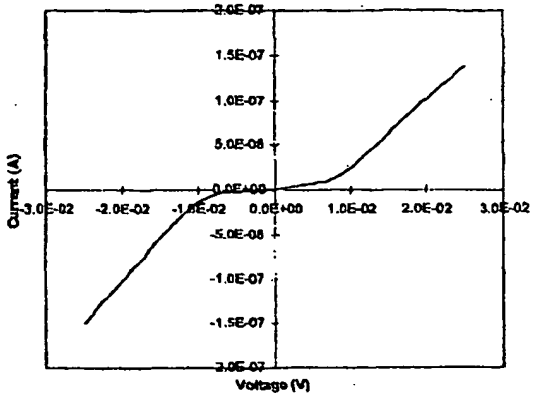


Fig. 2. Small signal I-V plot of large test structure (100 x 100 μm electrodes, 10 μm spacing, on unpatterned 150 nm thick $Ag_4As_2S_3$ layer).

Using the test array layout shown in schematic form in Fig. 3, small signal I-V measurements were performed on a wide variety of devices with device lengths and widths (defined in Fig. 1) ranging from 4 - 200 μm and 4 - 50 μm respectively. These were used to obtain the inverse slope of the I-V curves at zero volts, defined as the off resistance, $R_{off}$, of the devices. $R_{off}$ vs. device length for various device widths is plotted in Fig. 4. These results show that $R_{off}$ is a geometric function of the channel dimensions, following $R_{off} = \rho L/dW + R_p$, where $\rho$ is the resistivity of the layer and d is the thickness of the chalcogenide. $R_p$ is the effective resistance at zero channel length and is mainly due to electrode polarization. The slope of the curves in Fig. 4 show that the resistivity is in the mid $10^2$ Ω.cm range. The value of $R_p$ for these devices is in the $10^8$ to the low $10^9$ Ω range. Due to the particular electrode configuration used, it is difficult to express $R_p$ as a specific contact/polarization resistance, i.e., the electrodes are made large to facilitate electrical probe contact but the effective contact area exists only at the point where the channel starts and this is not easily defined. Measurements on devices which did have well defined contact areas revealed that $R_p$ was around $10^{10}$ Ω.μm$^2$.

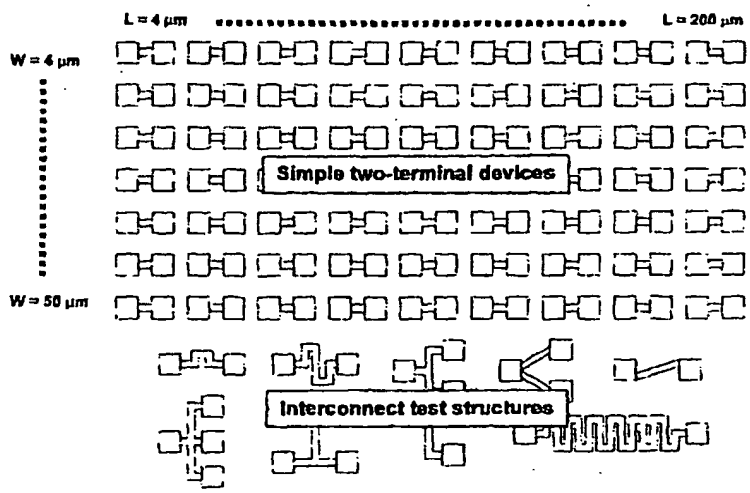


Fig. 3. Test array layout schematic for large geometry coplanar devices.

Fig. 5 is an example of constant current programming/switching of a broad (L = 6 μm, W = 50 μm) device. A Hewlett-Packard 4145 Semiconductor Parameter Analyzer was used as the current source and for measurement. The current used in this example was 50 nA (the applied voltage is varied automatically to maintain this current). Each

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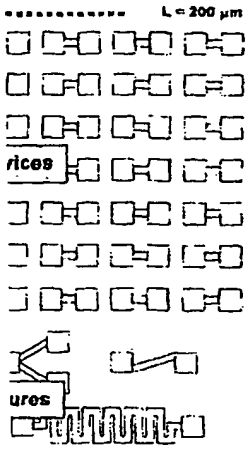


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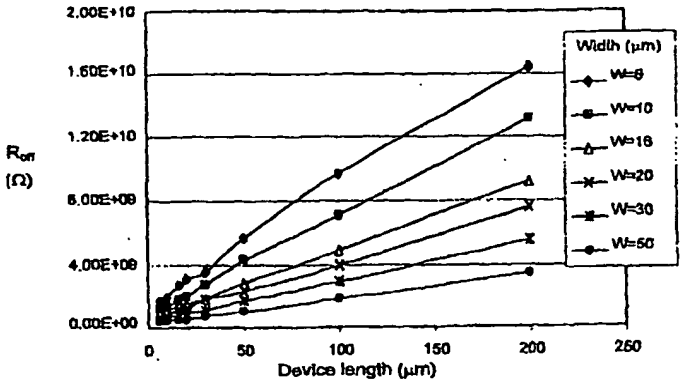


Fig. 4. Off resistance vs. device length for various device widths.

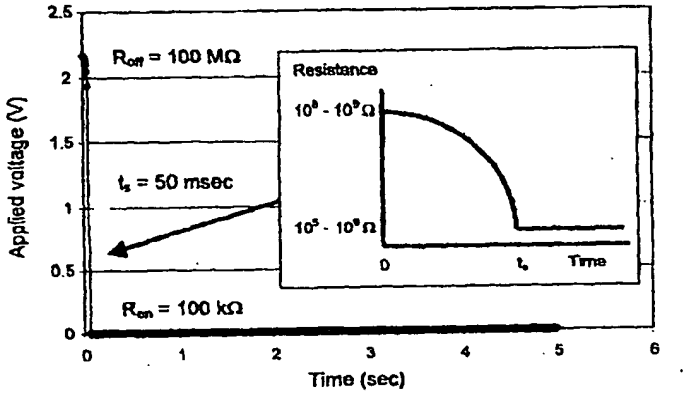


Fig. 5. Constant current (50 nA) programming of L = 6 μm, W = 50 μm device. The insert shows the general applied voltage vs. time trend for the devices tested.

data point is 10 msec apart. $R_{off}$ for this particular device (at zero applied voltage) is close to $10^8$ Ω but measured device resistance at t = 0 is around half this value when the forcing voltage is applied due to the exponential nature of the I-V characteristic (discussed earlier). The device attains a stable relatively low resistance state of around $10^5$ Ω after 50 - 60 msec, as indicated by the flat line portion of Fig. 5 along the x-axis. Scanning electron microscopy reveals that this lowered resistance is due to the presence of a narrow surface electrodeposit.

The "time-to-short", $t_s$, the time taken to grow the electrodeposit from cathode to anode, is found for constant current programming to be proportional to the device length and inversely proportional to the programming current, $i_p$. This is to be expected as the total volume of the electrodeposit depends on the total charge which flows in the device. The electrodeposition rate is therefore proportional to current so that a constant applied current produces a constant rate of electrodeposition. With a constant rate of growth, the time to short will depend linearly on the distance the electrodeposit has to bridge, i.e., the device length. Increasing the (constant) current applied will linearly increase the growth velocity and hence $t_s$ will be inversely proportional to current. The diagram in insert in Fig. 5 illustrates the general resistance vs. time trend for low constant current programming. The resistance typically decreases as

$$R(t) = (R_0 - Kt)R_C/[(R_0 - Kt) + R_C],$$

where $R_0 - Kt$ represents the resistance in the surface (electrodeposition) region, which decreases linearly with rate K Ω/sec from an initial value $R_0$ as the electrodeposit "short-circuits" the surface. $R_C$ is the relatively constant resistance value of the underlying film. Note that $R_0$ and $R_C$ cannot be measured directly and are therefore chosen to provide a best-fit model for any given set of data. R(t) is given by these two components in parallel and has the characteristic shown in Fig. 5. The energy, E, required to put the device in the low resistance state is given by the product of charge and voltage,

$$E = i_p \int_0^{t_s} V(t)dt = i_p^2 \int_0^{t_s} R(t)dt.$$

For the curve of Fig. 5, the total charge is 2.5 nC and the corresponding switching energy is approximately 3 nJ. If all the charge results in electrodeposition, this corresponds to $1.6 \times 10^{10}$ silver atoms. For a silver atomic density of $5.8 \times 10^{22}$ $cm^{-3}$, the total volume of the electrodeposit would be $2.7 \times 10^{-13}$ $cm^3$. Since the device length and hence electrodeposit length is 6 μm, the corresponding average cross-sectional area of the silver connection is $4.5 \times 10^{-10}$ $cm^2$ or $4.5 \times 10^4$ $nm^2$. However, the value of the on resistance suggests that if the electrodeposit is assumed to have the resistivity of bulk silver (in the order of $10^{-6}$ Ω.cm), the effective cross-sectional area is less than 1 $nm^2$. The more than three orders of magnitude discrepancy could be due to three factors; (1) a thin film resistivity which is considerably higher than the bulk silver value, (2) an inefficient electrodeposition process, or (3) an electrodeposit that has narrow regions which dominate the overall resistance. Surface effects do lead to considerably higher resistivities in thin films and so (1) is extremely likely. In addition, electron microscopy analysis suggests that the surface electrodeposits are generally somewhat uneven and so (3) is also likely to be a considerable factor in the increase of resistance.

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It should be noted that if the anode does not contain silver, the electrodeposition process does indeed become self-limiting and the resistance changes observed above are not attainable - in most cases the devices do not even produce a bridging electrodeposit. Also, as mentioned earlier, if the applied voltage is reversed during the growth, the electrodeposition process will reverse and the electrodeposit will dissolve back into the chalcogenide. However, an electrodeposit will form at the opposite electrode and this can also short-circuit the device. These devices must therefore be "erased", i.e., returned to a high resistance state, by the application of a current which is in excess of the current density which will cause failure in the electrodeposit. Care must be taken not to exceed the thermal limits of the device as excessive Joule heating will locally melt the electrolyte and render the device unusable. However, it has been shown that electrodeposits grown with sub-100 nA currents can be broken with 1 - 100 μA pulses of 1- 10 μsec duration without any apparent damage to the underlying chalcogenide. However, more work is required to establish the limits of the erase process and this is ongoing.

Fig. 6 shows the results from a number of 10 μm wide devices for a different type of programming, involving a 5 sec voltage sweep from 0.5 to 1.8 V with a 25 mA current limit. This produces a much more substantial surface electrodeposit with a resistance of around 1 Ω/μm of device length. The average contact resistance in this case is just under 10 Ω. Note that the stable low resistance state is attained when the applied voltage reaches 1.2 - 1.7 V. Below this range, there is no apparent stable electrodeposition and the device remains in the high resistance state. Note that the same trend and values were observed for a number of device widths over 10 μm as the electrodeposits did not cover the entire channel width at these dimensions and hence this parameter had no effect on the programmed resistance. Since the volume of the electrodeposit is dependent on the

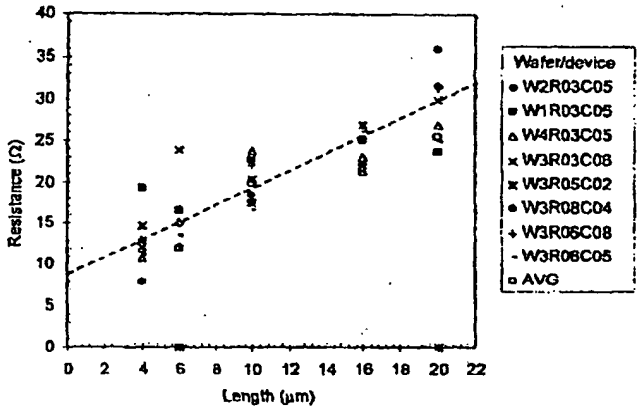


Fig. 6. Programmed resistance vs. length (10 μm wide) for a 0.5 - 1.8 V sweep with a 25 mA current limit.

total charge, it is reasonable to assume that a higher current limit will lead to a lower device resistance.

It should be noted that the electrodeposition process using constant current or voltage sweep (with current limit) programming is self limiting. This is due to the fact that as the resistance falls, the voltage drop across the electrodeposit will be determined by the current and the resistance. If this voltage is less than that required for electrodeposition, the process will halt. Voltage ramps from zero to 1.8 V on existing electrodeposits only result in further electrodeposition (up to the current limit) when the voltage is in excess of 300 mV. Below this, there is no further electrodeposition and the resistance remains at the value set by the original programming condition. For example, a device originally programmed with a voltage sweep with a 25 mA limit which attains a resistance of 18 Ω can be reduced to 10 Ω if the sweep is reapplied with a 100 mA limit.

## APPLICATIONS

We have seen that the electrodeposition process depends on a number of factors, including the magnitude of the applied voltage and current. Therefore, by appropriate choice of programming parameters, the metal electrodeposit may be grown so that it is relatively difficult to break. This characteristic is useful in applications such as the one time programmable (OTP) programmable read only memory (PROM) or as an anti-fuse circuit configuration element. Alternatively, by using a low writing current, the link may be formed with "weaknesses" so that it may be subsequently broken by a current pulse (or pulses) to erase the data. In either memory application, the information is stored as the presence or absence of the metallic link and the differences between logic states is large and therefore very easy to detect. Fig. 7 shows a micrograph of an antifuse PROM using PMC elements in the upper level of metallization and transistor cell isolation.

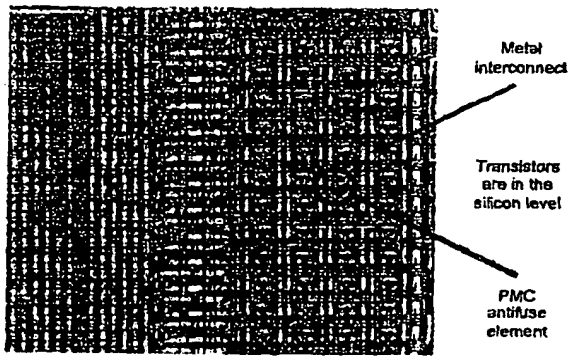


Fig. 7. Example of transistor isolated PMC antifuse PROM circuit.

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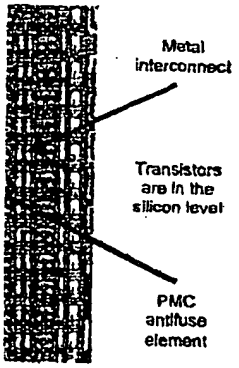


antifuse PROM circuit.

The ability to form interconnections in a complex 3-dimensional integrated circuit structure once fabrication has been completed is highly desirable as it allows an unprecedented level of flexibility in testing, debugging, and system reconfiguration. Such flexibility would be particularly useful in high reliability systems in aircraft or space vehicles. If programmable interconnections were available in these systems, defective circuitry could be tested using temporary probe connections, or signals could be rerouted around problem areas. A reconfigurable metallization scheme is possible using metal-doped chalcogenide elements as part of the interconnect. In a practical scheme, the metal-doped chalcogenide would be patterned in dielectric-separated layers in much the same way as metallization is in a traditional interconnect scheme. Prior to metal element growth, these pathways would have an extremely high resistance to current flow. To connect two points within the circuit, an appropriate voltage would be applied to either end of the selected pathway to stimulate metal growth. In the case of the arsenic trisulfide/silver system, silver features, several hundred microns long, may be grown in a few seconds on the surface of the doped chalcogenide, thereby connecting two widely-spaced circuit elements with a silver "wire". The interconnect pathways may have bends, vias, and branches (multiple in and multiple out) but the metal features will only grow between the points which have the voltage applied, thereby forming a controllable and directed electrical connection. The interconnect test structures shown in the lower half of Fig. 3 have allowed us to explore this possibility.

One of the greatest problems in deep-submicron circuits is the reliability of the metal interconnects. Small geometry interconnects are highly prone to failure by electromigration at points where the lines have a reduced cross-section due to thinning at topographical features (e.g., an underlying step), line narrowing by reflective notching during a photolithography step, and morphological effects such as width variations at grain boundaries after etching. Consequently, metal lines have to be made wider than the minimum lithographical linewidth, by a factor of two or more, to reduce the current density at thin regions and thereby reduce electromigration. The requirement for wider lines reduces the overall interconnect density. If interconnect metal is deposited on a thin layer of metal doped chalcogenide, a break or other high resistance region in the track would be "healed" by the formation of a metal element, formed by electrodeposition at the break. This would increase the overall system reliability as it would constitute an in-situ repair mechanism. Indeed, a break could be healed in any conductive track with an underlying layer of copper- or silver-doped chalcogenide as long as there was not an adverse reaction between the conductor and the doped glass. A schematic of a potential multi-level interconnect scheme is shown in Figure 8. In this scheme, all small geometry metal lines have a doped glass layer in contact with them. The figure shows the glass layer beneath the conductor but it could also be deposited on top or completely surround the metal line. The via regions would be kept free of the glass to minimize the resistance of the connection between interconnect layers. The mechanism responsible for the healing effect is the electrodeposition of metal from solid solution by the action of the potential difference across the defect region. As the weak region in the conducting track becomes thinner by electromigration, its resistance will increase and hence the voltage drop across it will increase. This potential difference will create an electric field which will move the dissolved metal ions to the most electrically negative part of the defect whereupon they will come out of solution and form a solid metal element at the surface

of the glass. The metal electrodeposit will grow until the defect is bridged, i.e., returned to a low resistance state. Note that this repair process is self regulating as it will only operate when the defect resistance becomes high and will "turn off" when the repair is complete. This is because the electrodeposition process requires a minimum potential drop of around 300 mV in order to proceed.

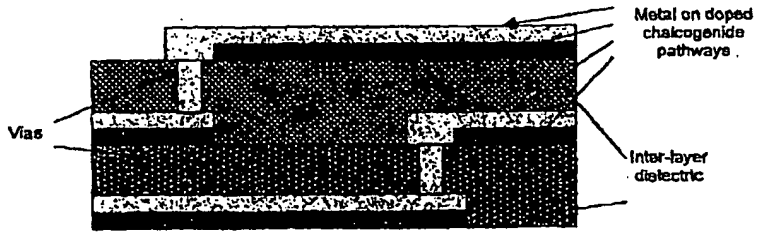


Fig. 8. Self-healing interconnect scheme.

## CONCLUSIONS

The Programmable Metallization Cell has been described in terms of its fundamental electrochemical/physical nature and its basic electrical characteristics. Silver may be photodissolved into arsenic trisulfide using u.v. light to form a solid solution. This process proceeds by cation reduction and self-limits when the arsenic reaches minimum valency at the composition $Ag_4As_2S_3$. The silver ions may be brought out of solution in the form of a surface electrodeposit in devices which consist of coplanar electrodes on a metal doped chalcogenide film. This electrodeposit, having a resistance which is many orders of magnitude lower than that of the solid solution, will result in a large resistance reduction between the terminals if it is grown completely from the cathode to the anode. The anode should contain a source of silver which dissolves into the chalcogenide during electrodeposition otherwise the electrodeposit will likely not bridge the anode-cathode gap. The electrodeposition process can be reversed by reversing the polarity of the applied voltage. It would appear to be more practical to make the device "erasable", i.e., able to be returned to a high resistance state, by first growing a "weak" electrodeposit that can be broken with a current pulse which is low enough so as not to damage the underlying electrolyte.

The off resistance of the devices is determined by device geometry and the polarization resistance of the contacts. The on resistance depends on the amount of charge which is applied which in turn depends on the programming current. For the devices tested, constant current programming at very low currents (less than 100 nA) produced a resistance change from more than $10^9$ Ω down to around $10^5$ Ω with energy consumption in the nJ range. Voltage sweep programming with high current limit (25 mA) produced on resistances of approximately 1 Ω/μm of device length with a contact resistance in the order of 10 Ω. Reprogramming these devices with a higher current limit, e.g., 100 mA, produced considerably lower resistance through additional

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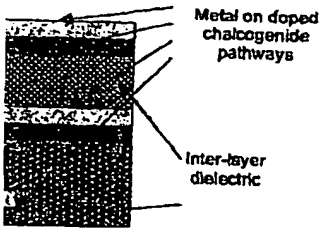


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electrodeposition. This "thickening" of the electrodeposit will only occur when the applied voltage reaches 300 - 400 mV.

The electrodeposition effect and the ensuing resistance changes at low voltage and energy will have utility in a diverse range of applications which include non-volatile memories, anti-fuses, programmable interconnects, and self healing metallization.

This work was supported by Axon Technologies Corporation.

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